WHAT IS CLAIMED IS

1. A semiconductor device comprising a plurality of stages of voltage booster circuits for potentially raising a power supply voltage up to a predetermined final output voltage, an output voltage control means connected to a voltage booster circuit adjacent to a final stage of said voltage booster circuits, and an internal element to which an output of said voltage booster circuits is supplied, wherein a first stage voltage booster circuit of said voltage booster circuits for raising the power supply voltage up to a primary voltage is formed of a converter circuit including an inductance element, a switching element and a diode, wherein voltage booster circuits in back of the first stage for raising said primary voltage up to the predetermined final voltage are each configured from a charge pump circuit including a capacitance element and a diode or a converter circuit including an inductance element, a switching element and a diode, wherein the inductance element and the switching element plus the diode making up said voltage booster circuit as well as said output voltage control means and said internal element are formed on a semiconductor substrate, and wherein said output voltage control means controls the voltage booster

circuit near said final stage and supplies its output to said internal element.

2. A semiconductor device comprising a plurality of stages of voltage booster circuits for potentially raising a power supply voltage up to a predetermined final output voltage, an output voltage control means connected to a voltage booster circuit near a final stage of said voltage booster circuits, and an internal element to which an output of said voltage booster circuits is supplied, wherein a first stage voltage booster circuit of said voltage booster circuits for raising the power supply voltage up to a primary voltage is formed of a charge pump circuit including a capacitance element and a diode, wherein any one of voltage boost stages in back of the first stage for raising said primary voltage up to the predetermined final voltage is configured from a converter circuit including an inductance element, a switching element and a diode, wherein the inductance element and the switching element plus the diode making up said voltage booster circuit as well as said output voltage control means and said internal element are formed on a semiconductor substrate, and wherein said output voltage control means controls the voltage booster circuit near said final stage and supplies its

output to said internal element.

3. The semiconductor device according to claim 2, wherein a voltage boost ratio of said first stage voltage booster circuit is less than that of a converter circuit at a succeeding location of said first stage.

4. The semiconductor device according to claim 1, wherein said power supply voltage is less than or equal to 2.5V.

5. The semiconductor device according to claim 1, wherein at least one converter circuit of said converter circuits is such that its voltage boost ratio is maintained at a preset value during a voltage boosting operation.

6. The semiconductor device according to claim 1, further comprising means for causing, in at least one converter circuit of said converter circuits, a voltage boost ratio to be retained at a preset value during a voltage boost operation and for arbitrarily setting the voltage boost ratio.

7. The semiconductor device according to claim 1, wherein at least one converter circuit of said converter circuits is such that a switching duty ratio is kept at a preset value during a voltage boost operation.

8. The semiconductor device according to claim 1, wherein at least one converter circuit of said converter circuits is 10 MHz or more in its switching frequency.

9. The semiconductor device according to claim 1, wherein said inductance element is a parallel connection type inductance element consisting essentially of multilayered metal wiring layers and a dielectric film provided between the wiring layers, with said multilayered metal wiring layers being connected in parallel.

10. The semiconductor device according to claim 9, wherein a metal wire forming said inductance element is a spiral-shaped wiring line, wherein said spiral-shaped wiring line has an outer peripheral end connected to a wire for supplying said power supply voltage and also has an inner peripheral end connected via a metal wire to a diffusion layer of said switching element as formed in an element area beneath an inductance element.

11. The semiconductor device according to claim 1, wherein said internal element operable upon application of a voltage higher than the power supply voltage is a non-volatile memory.

12. A memory card using the semiconductor device

according to claim 1.

13. A semiconductor device comprising:

a plurality of stages of voltage booster circuits for raising a power supply voltage up to a prespecified final output voltage;

a voltage control unit connected to more than one voltage booster circuit within said plurality of stages of voltage booster circuits for controlling an output voltage near a final stage; and

an internal element to which the final output voltage is supplied from said plurality of stages of voltage booster circuits, wherein

a converter circuit provided within said plurality of stages of voltage booster circuits at least has an inductance element, a switching element, a diode and a driver circuit for driving said switching element, and

said inductance element of said converter circuit at least includes a metal wire to be formed at the same time during formation of either a signal wire of said internal element or a metal wire used for power supply wiring.

14. The semiconductor device according to claim 13, wherein said inductance element is a parallel-connection type inductance element with multilayered metal wires being connected in parallel.

15. A memory card using the semiconductor device according to claim 13.

16. The semiconductor device according to claim 14, wherein said semiconductor device is any one of a flash memory and a flash memory-embedded microcomputer.

17. The semiconductor device according to claim 14, wherein said multilayered metal wires making up said inductance element are such that central points of respective areas of respective metal wires forming an inductance element upon overlapping of projection images thereof are within areas of mutually different metal wires.

18. A multi-chip type semiconductor device comprising a plurality of semiconductor devices each including a plurality of stages of voltage booster circuits for potentially raising a power supply voltage up to a final output voltage, a voltage control unit connected to more than one voltage booster circuit within said plurality of stages of voltage booster circuits for controlling an output voltage near a final stage, and an internal element to which the final output voltage is supplied from said plurality of stages of voltage booster circuits, and also including within said plurality of stages of voltage booster circuits a converter circuit at least

having an inductance element, a switching element, a diode and a driver circuit for driving said switching element while letting said inductance element of said converter circuit include at least a metal wire as formed by the same process as either a signal wire of said internal element or a metal wire used for power supply wiring, wherein

said plurality of semiconductor devices are disposed to overlap respectively, and wherein the inductance elements within neighboring ones of said semiconductor devices are laid out in such a manner as to prevent inductance elements within the semiconductor devices from mutually overlapping in directions lying immediately above and below said inductance elements.

19. The multi-chip type semiconductor device according to claim 18, wherein said plurality of semiconductor devices are formed on a semiconductor chip, and wherein said inductance element of said semiconductor device is formed at one half side part of the semiconductor chip whereas the inductance element of another semiconductor device lying next to said semiconductor device is at a remaining half side part of the chip.

20. The multi-chip type semiconductor device

according to claim 18, wherein said inductance element is a parallel connection type inductance element with a parallel connection of multilayered metal wiring layers.

21. The multi-chip type semiconductor device according to claim 18, wherein said semiconductor device is a flash memory or a flash memory-embedded microcomputer.

22. The multi-chip type semiconductor device according to claim 18, wherein said multilayered metal wires making up said inductance element are such that central points of respective areas of respective metal wires forming an inductance element upon overlapping of projection images thereof are within areas of mutually different metal wires.

23. A semiconductor device comprising:

a plurality of stages of voltage booster circuits for potentially raising a power supply voltage up to a final output voltage;

a voltage control unit connected to more than one voltage booster circuit within said plurality of stages of voltage booster circuits, for controlling an output voltage near a final stage; and

an internal element to which the final output voltage is supplied from said plurality of stages of

voltage booster circuits, wherein

a first stage voltage booster circuit within said plurality of stages of voltage booster circuits has a converter circuit having an inductance element, a switching element, a diode, and a driver circuit for driving said switching element, and

said switching element and said diode of said converter circuit are partly disposed to underlie said inductance element.

24. A semiconductor device comprising:

a voltage step-down circuit for potentially reducing an input voltage to a final output voltage, wherein

said voltage step-down circuit has a converter circuit having an inductance element, a switching element, a diode, a driver circuit for driving said switching element, and a control circuit for control of an output voltage, and

said switching element and said diode of said converter circuit are partially laid out to underlie said inductance element.

25. The semiconductor device according to claim 23, further comprising:

a spirally wired first metal wire for forming said inductance element;

a second metal wire connected to an outer periphery end of said first metal wire for supplying said power supply voltage;

an interlayer connection wire connected to an inner periphery end of said first metal wire while being wired from said inner periphery end toward underlying diffusion layers of said switching element and said diode; and

a third metal wire for connection between the diffusion layers of said switching element and said diode.

26. The semiconductor device according to claim 24, said device has a first metal wire as spirally wired to form said inductance element, an interlayer connection wire connected to an inner periphery end of said first metal wire while being wired from said inner periphery end toward underlying diffusion layers of said switching element and said diode, a third metal wire for connection between the diffusion layers of said switching element and said diode, and a fourth metal wire connected to an outer periphery end of said first metal wire for outputting said final output voltage thus reduced in potential.

27. The semiconductor device according to claim 23, wherein said switching element and said diode are

laid out on a semiconductor substrate so that a drain-side region of said switching element and an anode-side region of said diode oppose each other, thereby having a configuration including a parallel connection of at least two or more sets of combination units of switching elements and diodes with both regions electrically coupled together.

28. The semiconductor device according to claim 24, wherein said switching element and said diode are laid out on a semiconductor substrate so that a source-side region of said switching element and a cathode-side region of said diode oppose each other, thereby a configuration including a parallel connection of at least two or more sets of combination units of switching elements and diodes with both regions electrically coupled together.

29. The semiconductor device according to claim 23, wherein said inductance element is such that a plurality of layers each having said first metal wire and an inter-wiring layer dielectric film are connected in parallel.

30. The semiconductor device according to claim 23, wherein said semiconductor device is any one of a nonvolatile memory and a nonvolatile memory-embedded microcomputer.

31. The semiconductor device according to claim 30, wherein said nonvolatile memory or said nonvolatile memory-embedded microcomputer is a flash memory or a flash memory-embedded microcomputer.

32. A multi-chip type semiconductor device comprising a plurality of semiconductor devices each including a plurality of stages of voltage booster circuits for potentially raising a power supply voltage up to a final output voltage, a voltage control unit connected to more than one voltage booster circuit within said plurality of stages of voltage booster circuits for controlling an output voltage near a final stage, and an internal element to which the final output voltage is supplied from said plurality of stages of voltage booster circuits, wherein a first stage voltage booster circuit within said plurality of stages of voltage booster circuits has a converter circuit having an inductance element, a switching element, a diode and a driver circuit for driving said switching element, and wherein said switching element and said diode of said converter circuit are partly disposed to underlie said inductance element, wherein said plurality of semiconductor devices are disposed to overlap respectively, and wherein said inductance elements

within neighboring ones of said semiconductor devices are laid out in such a manner as to prevent said inductance elements within other semiconductor devices from mutually overlapping in directions immediately above and beneath said inductance elements.

33. The multi-chip type semiconductor device according to claim 32, wherein said plurality of semiconductor devices are formed on a semiconductor chip, and wherein said inductance element of said semiconductor device is formed at part of on half side of the semiconductor chip whereas an inductance element of another semiconductor device neighboring upon said semiconductor device is formed at part of a remaining half side of the chip.

34. The multi-chip type semiconductor device according to claim 32, wherein each of said plurality of semiconductor devices is a nonvolatile memory or a nonvolatile memory-embedded microcomputer.

35. The multi-chip type semiconductor device according to claim 32, wherein said nonvolatile memory or said nonvolatile memory-embedded microcomputer is a flash memory or a flash memory-embedded microcomputer.